

A New Fabrication Process for Planar Thin-Film Multijunction Thermal Converters

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Abstract—Advanced thin-film processing and packaging technologies are employed in the fabrication of new planar thin-film multijunction thermal converters (MJTCs). The processing, packaging, and design features build on experience gained from prior NIST demonstrations of thin-film converters and are optimized for improved sensitivity, bandwidth, manufacturability, and reliability.

Index Terms—AC-DC transfer, metrology, standard, thermal converter, voltage.

I. INTRODUCTION

RECENT efforts at the National Institute of Standards and Technology (NIST) and the Physikalisch-Technische Bundesanstalt (PTB), have focused on developing novel designs of multijunction thermal converters (MJTCs) in thin-film fabrication technologies [1], [2]. Thin-film design and construction shows promise for producing a large number of high-quality MJTCs at relatively low cost. The most significant advantage of the thin-film device is that the difficulties encountered in manual construction of conventional wire MJTCs are completely replaced by highly reproducible metal sputtering, photolithographic patterning, and subsequent etching. Despite many advances, a number of difficulties remain in producing thin-film thermal converters.

A thin-film MJTC (see Fig. 1) is comprised of a resistive heater and proximately placed thermocouples that sense any difference in temperature between dc and ac excitation. The heater and thermocouple hot junctions are constructed on a thin-film dielectric membrane that provides thermal isolation from the substrate. In this paper, new processing and vacuum packaging methods will be described. These methods alleviate some of the inherent difficulties in fabrication. Specifically, a description is given of the following:

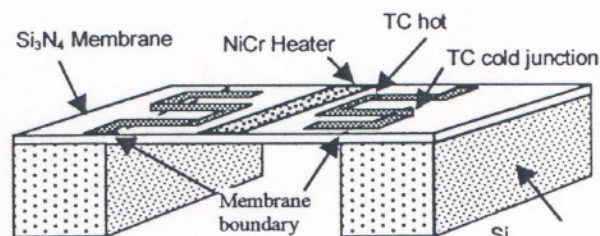


Fig. 1. Schematic representation of the essential features of a thin-film thermal converter.

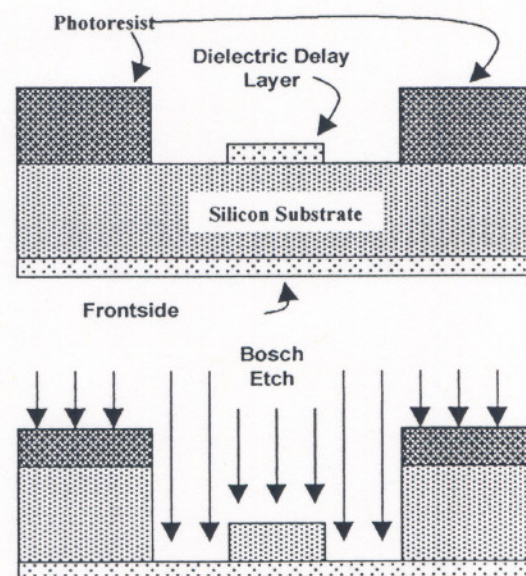


Fig. 2. Patterned backside "delay" layer (top) and resulting silicon obelisk (bottom).

- 1) a low-stress silicon-nitride dielectric membrane;
- 2) a lift-off technique for improved feature patterning;
- 3) a new Bosch¹ etching process employed for back-etching of the membrane and definition of a silicon obelisk;
- 4) an advanced vacuum packaging method.

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¹Identification of commercial equipment, instruments, and/or materials does not imply recommendation or endorsement by NIST or Sandia, nor does it imply that the material or equipment identified is necessarily the best available for the specified purpose.

II. THERMAL CONVERTER FABRICATION

The heater structure is optimized through numerical thermal simulation and designed to provide a uniform temperature distribution across the central region where 100 thermocouple pairs are connected in series. The heater is of NiCrAlCu alloy ($w_{Cr} = 0.2$, $w_{Al} = 0.025$, $w_{Cu} = 0.025$)² for voltage converters. This alloy composition results in thermoelements with a very low temperature coefficient of resistance on the order of $10 (\mu\Omega/\Omega)/^\circ\text{C}$. Thermoelements with gold heaters are also constructed for use as current converters. The use of gold as the heater, bond-wire, and package lead material completely eliminates any Peltier heating in the device. All devices fabricated use thermocouples of CuNi alloy ($w_{Ni} = 0.45$) for the negative leg and NiCr alloy ($w_{Cr} = 0.1$) for the positive leg. The Seebeck coefficient for a thermocouple pair is approximately $65 \mu\text{V}/^\circ\text{C}$. Gold bond pads are formed at the input/output of the heater and at the ends of the multijunction thermocouple bank.

The use of sputtered metals provides uniformity in composition of the deposited thin-film thermocouples and heater. Wet chemical etching steps are eliminated through the use of a photoresist lift-off. This technique, widely utilized for evaporated metals, results in well-defined features and a reduction in processing steps.

III. BACKSIDE PROCESSING

Among the troublesome difficulties in fabrication is the production of the freestanding dielectric membrane. Silicon dioxide and silicon nitrides are known to produce high-stress thin films. The stress in these films is often enough to cause breakage on formation of the freestanding membrane by wet chemical back etching. Previous designs have used a "sandwich" oxide/nitride/oxide deposition to compensate for the internal stress of the nitride dielectric [1], [2]. This approach has been successful in improving yield over single layer oxide or nitride dielectric approaches. In this study, we propose a simpler technique employing commercially available silicon substrates with a 5000 Å low-stress nitride film followed by a Bosch etch (described below). The improved yield implies that this method has produced stronger freestanding membranes than the more complicated dielectric sandwich membrane technique.

Removal of silicon below the heater and thermocouple hot junctions provides a thermally isolated membrane and is the key step in producing a thermal converter. Following patterning, a deep reactive ion etching process (DRIE) is employed. The patented DRIE process [3] utilizes an iterative inductively coupled plasma-based deposition/etch cycle in which a polymer etch inhibitor is conformally deposited over the wafer during the deposition cycle. The polymer deposits over the resist mask, the exposed silicon field, and along the sidewall of the feature to be etched. The polymer film is preferentially sputtered from the bottom of the silicon trench. The polymer film on the sidewall is removed at a much slower rate, minimizing lateral etching of the silicon.

²Alloy compositions are noted as follows: the primary alloy constituent is noted first and w_B is the mass fraction of the alloy constituent B .

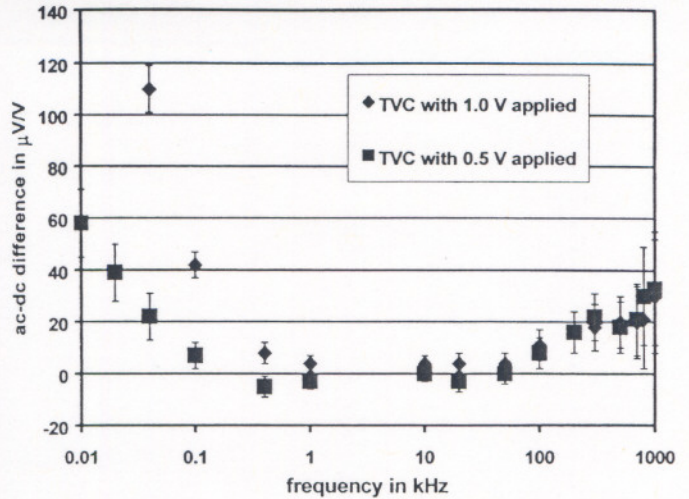


Fig. 3. Results for a thin-film MJTC with a 980 Ω heater at 0.5 V and 1.0 V applied.

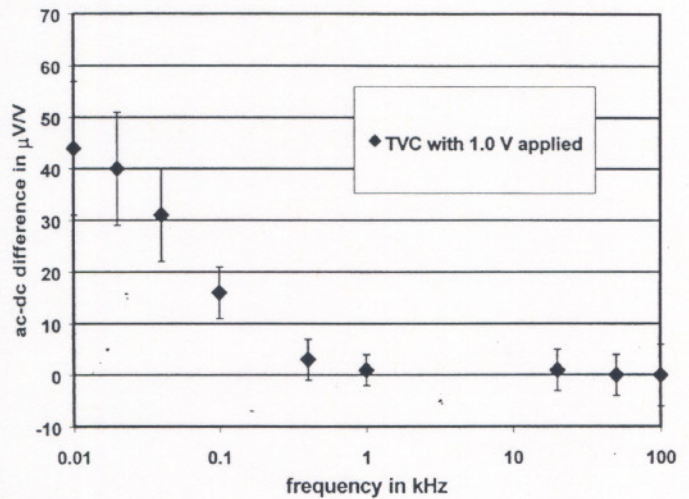


Fig. 4. Improvement in low-frequency ac-dc difference for thin-film MJTCs with obelisk and longer time constants.

A silicon obelisk may be formed to increase the thermal time constant, as shown in Fig. 2. A sacrificial dielectric layer is patterned beneath the heater. The dimensions of the patterned dielectric delay layer determine the lateral geometry of the obelisk. The relative etch ratio of the Bosch DRIE process for Si:Si₃N₄ and the thickness of the Si₃N₄ allows control of the vertical geometry. Adjustment of the thickness of the dielectric layer can be made to optimize the thermal time constant.

IV. VACUUM PACKAGING

Under vacuum, thermal converters exhibit an increase in sensitivity and an increase in thermal time constant. An advanced vacuum packaging process is employed in sealing the fabricated devices in a leadless chip carrier (LCC) ceramic package under vacuum. The process utilizes a commercial high vacuum hermetic sealer and film getters composed of a NiCr ribbon covered with a porous mixture of Ti and Zr-V-Fe alloy [4]. The getters are soldered to the package lids and allow the vacuum

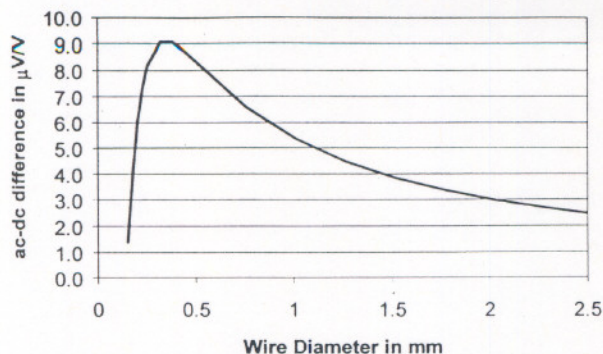


Fig. 5. Computed estimate of skin effect for gold lead-in wire at 1 MHz.

in the package to be maintained below levels where convective heat loss is significant.

V. PERFORMANCE CHARACTERISTICS

Several thermal converters have been compared against NIST and Sandia working standards. The new process has produced devices with low ac-dc differences and high sensitivities. As an example, a set of data taken at 0.5 V and 1.0 V is shown in Fig. 3 for a 980 Ω thermal voltage converter (TVC). The short thermal time constants produce significant low frequency errors that are reduced in thermal converters with the obelisk (Fig. 4). The device shown in Fig. 3 has been optimized for performance to 1 MHz.

A. High-Frequency Performance

Testing of initial devices assembled in conventional thermal converter housings showed significant skin effect error at 1 MHz. Upon reassembly of the devices in coaxial housings with much thinner lead wire, the ac-dc differences of the film MJTCs due to skin effect and capacitive losses were seen to be reduced from over 30 $\mu\text{V/V}$ to less than 10 $\mu\text{V/V}$. The estimated contribution to the ac-dc difference caused by skin effect in various sizes of wire is shown in Fig. 5.

B. Low-Frequency Performance

Three dimensional finite-element thermal models were developed to optimize the heater geometry and the thermocouple

layout, and to compute the increase in thermal time constant due to the silicon obelisk. A significant low-frequency error is present for devices operated under dry nitrogen. It is likely that further optimization and/or thermal compensation will be required in order to fully achieve the capabilities of the thin-film device in this frequency regime.

VI. CONCLUSIONS

A new fabrication process for thin-film multijunction thermal converters has been developed. The new process has some distinct advantages over previous methodology. In particular, a number of wet chemical steps utilized in the patterning of the frontside metal layers, backside etch cavity, and silicon obelisk have been replaced with dry processes. A more robust method of forming a dielectric membrane has been demonstrated resulting in enhanced yield and higher temperature capability.

Of particular significance, are the results obtained above 100 kHz. Reduced ac-dc differences over previous work are demonstrated in this higher frequency regime. Additional work is necessary to develop a single device that will span the low and high frequency ranges.

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